WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device comprising the steps of:

forming a lower wiring layer on a semiconductor substrate;

coating two or more layers of dielectric films over the lower wiring layer;

forming a via hole and a groove through the dielectric films; and

forming an upper wiring layer in the groove and a via in the via hole to connect the lower wiring layer with the upper wiring layer,

wherein the maximum process temperature $T_{process\_max}$ after forming the dielectric films is determined using following inequality (1):

$$(\alpha - \alpha'_{diel})\frac{E}{1-\nu}(T_{process\_max} - T) \leqq A \qquad (1),$$

where A represents critical stress value near the via, which is predetermined as a critical value causing voids near the via by a thermal treatment after forming the dielectric films,

α represents a thermal expansion coefficient of the via and the upper wiring layer;

α'_{diel} represents an average thermal expansion coefficient of the dielectric films calculated with their relative thickness;

E represents an elastic coefficient of the via and the upper wiring layer;

ν represents a Poisson's ratio of the via and the upper wiring layer; and

T represents a stress relaxation temperature of the via and the upper wiring layer.

2. A method for fabricating a semiconductor device according to Claim 1,

wherein the upper wiring layer and the via are made of metal.

3. A method for fabricating a semiconductor device according to Claim 2,

wherein the upper wiring layer and the via are made of copper, and

the maximum process temperature is determined according to the inequality (1) using T=300 ℃ and A=200 MPa.

4. A method for fabricating a semiconductor device according to Claim 2,

wherein the upper wiring layer and the via are made of copper, and

the maximum process temperature $T_{process\_max}$ is equal to or lower than 450 ℃.

5. A method for fabricating a semiconductor device comprising the steps of:

forming a lower wiring layer on a semiconductor substrate;

coating one or more layers of dielectric films over the lower wiring layer;

forming a via hole and a groove through the dielectric films; and

forming an upper wiring layer in the groove and a via in the via hole to connect the lower wiring layer with the upper wiring layer,

wherein combination of materials of the dielectric films and relative thickness of the dielectric films are determined based on α'_{diel} calculated by following inequality (2):

$$(\alpha - \alpha'_{diel})\frac{E}{1-\nu}(T_{process\_max} - T) \leq A \qquad (2),$$

where A represents critical stress value near the via, which is predetermined as a critical value causing voids near the via by thermal treatment after forming the upper wiring layer,

α represents a thermal expansion coefficient of the via and the upper wiring layer;

α'_{diel} represents an average thermal expansion coefficient of the dielectric films calculated with their relative thickness;

E represents an elastic coefficient of the via and the upper wiring layer;

ν represents a Poisson's ratio of the via and the upper wiring layer;

$T_{process\_max}$ represents maximum process temperature of the semiconductor device after forming the upper wiring layer; and

T represents a stress relaxation temperature of the via and the upper wiring layer.

6. A method for fabricating a semiconductor device according to Claim 5,

wherein the upper wiring layer and the via are made of metal.

7. A method for fabricating a semiconductor device according to Claim 6,

wherein the upper wiring layer and the via are made of copper, and

the combination of materials of the dielectric films and the relative thickness of the dielectric films are determined based on α'_{diel} calculated by the inequality (2) using T=300 ℃ and A=200 MPa.

8. A method for fabricating a semiconductor device according to Claim 6,

wherein the upper wiring layer and the via are

made of copper, and

the maximum process temperature $T_{process\_max}$ is equal to or lower than 450 ℃.

9. A semiconductor device comprising:

a lower wiring layer formed on a semiconductor substrate;

two or more layers of dielectric films formed over the lower wiring layer;

a via hole and a groove provided through the dielectric films;

an upper wiring layer formed in the groove; and

a via formed in the via hole to connect the lower wiring layer with the upper wiring layer,

wherein the maximum process temperature $T_{process\_max}$ after forming the dielectric films or materials of the dielectric films and relative thickness of the dielectric films are determined using following inequality (3):

$$(\alpha - \alpha'_{diel})\frac{E}{1-\nu}(T_{process\_max} - T\ ) \leqq A \qquad (3),$$

where A represents critical stress value near the via, which is predetermined as a critical value causing voids near the via by a thermal treatment after forming the dielectric films,

α represents a thermal expansion coefficient of the via and the upper wiring layer;

α'_{diel} represents an average thermal expansion

coefficient of the dielectric films calculated with their relative thickness;

E represents an elastic coefficient of the via and the upper wiring layer;

ν represents a Poisson's ratio of the via and the upper wiring layer; and

T represents a stress relaxation temperature of the via and the upper wiring layer.

10. A semiconductor device according to Claim 9,

wherein the upper wiring layer and the via are made of metal.

11. A semiconductor device according to Claim 10,

wherein the upper wiring layer and the via are made of copper, and

the maximum process temperature is determined according to the inequality (1) using T=300 ℃ and A=200 MPa.

12. A semiconductor device according to Claim 10,

wherein the upper wiring layer and the via are made of copper, and

the maximum process temperature $T_{process\_max}$ is equal to or lower than 450 ℃.

13. A semiconductor device according to Claim 9,

at least one layer of the dielectric films is made of ladder-oxide.

14. A semiconductor device according to Claim 13, at least one layer of the other dielectric films is made of SiC.